SURFACE PATTERNING

Ancients inspire modern memory

A stencilling technique for depositing arrays of nanoscale ferroelectric capacitors on a surface could be useful in data storage devices.

J. Marty Gregg
is in the Department of Physics and Astronomy, Queen's University, Belfast BT7 1NN, Northern Ireland.
e-mail: m.gregg@qub.ac.uk

Figure 1 Hand stencils have survived on the walls of caves for tens of thousands of years, storing information about who was there. Researchers are developing data-storage techniques that are also based on stencilling.

Even in Palaeolithic times, people used stencils to help with data storage. Throughout the world, spray-painted stencils of human hands on the walls of caves have recorded who was there and acted as signatures for those who were responsible for the art on the walls (Fig. 1). It is remarkable that, thousands of years later, stencil patterning is now being proposed as a viable technology for the creation of electronic memory systems. On page 402 of this issue, Woo Lee and co-workers in Germany and Korea report a stencilling method to create a high-density array of ferroelectric nanocapacitors that could be used in ferroelectric random access memory (FeRAM) chips[1].

Stencilling provides an extremely low-cost option for nanoscale patterning and does not result in the kind of side-wall damage commonly associated with the physical bombardment or chemical attack methods used in conventional 'top-down' lithographic techniques. Such damage appears to be particularly detrimental to ferroelectric devices[2], making the stencilling approach for FeRAM shown by Lee and co-workers potentially extremely important.

Fabricating suitable templates or masks is central to all forms of stencilling. Lee and colleagues — who are based at the Max Planck Institute for Microstructure Physics, the Pohang University of Science and Technology and the Korea Research Institute of Standards and Science — started by electrochemically anodizing the surface of high-purity aluminium sheets to create thin films of porous aluminium oxide in which pseudo-regular arrays of nanoscale holes form naturally. The clever step was to spin-coat a layer of polystyrene on top of the aluminium oxide to act as a support for subsequent handling (see Fig. 1a in the Letter on page 403). This robust template was placed on top of a platinum-coated magnesium oxide substrate and the polystyrene support was removed before thin films of lead zirconium titanate — a common ferroelectric material — and then platinum were deposited through the holes of the stencil by pulsed laser deposition. The stencil was removed to reveal an array of nanoscale metal/ferroelectric/metal capacitor islands with diameters of ~60 nm. The distance between the centres of neighbouring islands was about 100 nm, giving a density of more than 10^{11} capacitors per square inch.

To appreciate the importance of this work, we must understand how ferroelectrics are used within the memory industry. FeRAM relies on two of the defining characteristics of ferroelectrics: first, the fact that their crystal structure leads to a spatial separation of positive and negative charge, known as a dipole; second, application of an external voltage can reverse the relative positions of these charges. When ferroelectrics are used in capacitors and integrated into FeRAM electrical circuits, the charge redistribution associated with this reversal or switching results in an obvious and measurable injection of current (Fig. 2). The presence or absence of a switching current reveals the original orientation of the dipole and can therefore be used to represent ones and zeroes.

Ferroelectric data storage is usually described as a developing technology even though it has already been used in, for example, games consoles and public transport smart card ticketing systems[3]. These applications require only relatively low bit densities, but the fundamental properties of ferroelectrics mean that much higher densities are possible. Previous research with continuous ferroelectric thin films has shown that memory can be written and remain stable down to individual bit diameters of ~5 nm (ref. 4), resulting in densities of more than 10^{13} bits per square inch. However, with few exceptions[5], such demonstrations have used 'moving parts' techniques such as scanning probe microscopy (SPM) to both write and read the data. Whereas SPM-based memory could lead to commercial devices through improvements using the 'millipede'

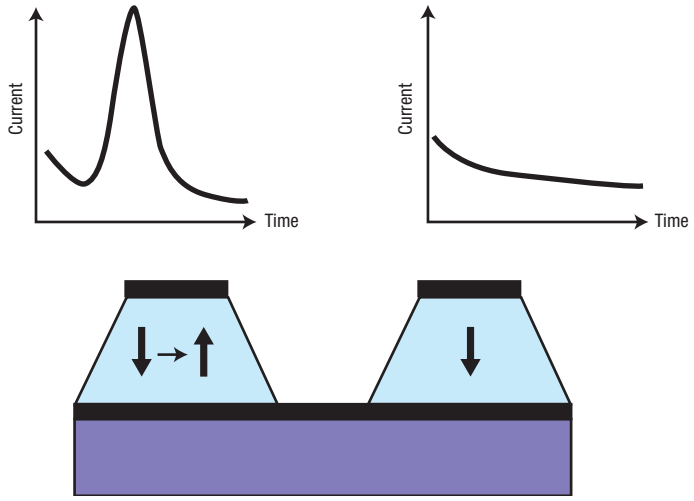

Figure 2 The electric dipoles in the ferroelectric layers (pale blue) of the nanocapacitors built by Lee *et al.* can point up or down, and can be switched by applying a voltage of the correct polarity to the upper electrode (left). When this happens, a distinct peak is measured in the current through the device. However, when the dipole is already aligned with the applied voltage, the current does not contain any distinctive features (right).

approach, current FeRAM technology is based on hard-wired arrays of individually addressable ferroelectric capacitors without any moving parts. The high-density arrays of individual capacitors fabricated by Lee and co-workers are capable of developing the 'no-moving-parts' approach to much higher densities than are currently available.

By creating ferroelectric nanocapacitors that are discrete, their performance as bit storage elements is improved and becomes more like those of bulk crystals than conventional thin films[6]. Such 'bit isolation' focuses the electric field — lessening the likelihood of cross-talk — and creates a physical barrier to the coarsening of ferroelectric domains, which removes the effects of the voltage or pulse duration on switching operations[7].

Impressive though the progress reported by Lee and co-workers is, there is still more work to do. If self-assembly is to make a dramatic impact in device manufacturing, we must learn how to hard-wire connections to arrays of nanoscale objects that are not perfectly ordered. In the context of FeRAM, continuous reductions in the size of individual capacitors cannot continue indefinitely: there is a limit to the size of switching current that can be accurately measured using sense amplifiers, and the current is proportional to the area of the electrodes in the capacitor structures. Thus, increases in areal bit densities — without reductions in the areas of individual electrodes — will be needed and will eventually require a move from planar two-dimensional to more complex three-dimensional architectures. But this is a Pandora's box that will wait for another day.

References

1. Lee, W. *et al. Nature Nanotech.* **3,** 402–407 (2008).
2. Stanishevsky, A. *et al. J. Appl. Phys.* **92,** 3275–3278 (2002).
3. Scott, J. F. *Science* **315,** 954–959 (2007).
4. Cho, Y., Hashimoto, S., Odagawa, N., Tanaka, K. & Hiranaga, Y. *Nanotechnology* **17,** S137–S141 (2006).
5. Evans, P. R. *et al. Nano Lett.* **7,** 1134–1137 (2007).
6. Nagarajan, V. *et al. Nature Mater.* **2,** 43–47 (2003).
7. Tybell, T., Paruch, P., Giamarchi, T. & Triscone, J.-M. *Phys. Rev. Lett.* **89,** 097601 (2002).

NANOELECTRONICS

The strain of it all

Electron interferometry can be used to measure strain with nanoscale resolution in electronic devices by exploiting a simple idea found in physics textbooks.

Abbas Ourmazd
is in the Department of Physics, University of Wisconsin Milwaukee, Wisconsin 53211, USA.
e-mail: ourmazd@uwm.edu

As in life, stress is ubiquitous in nanotechnology, and it rears its ugly head with monotonous regularity. Engineers respond with imaginative names for the consequences. For instance, the gaps that are left behind when stress causes chunks of material to disappear from the interconnects in an integrated circuit are known as 'rat bites'. However, again as can happen in life, a period of mutual respect has led to love: stress can now be used to 'hot-rod' microelectronic devices, and engineers are keen to get a look. Writing in *Nature*, Martin Hÿtch and co-workers[1] at the CEMES–CNRS laboratory in Toulouse provide powerful spectacles for this task.

One of the first lessons learned by microelectronic device pioneers in the 1950s was that many of the steps used to process semiconductors inevitably produce stress in the fabric of the devices. Diffusing phosphorous to form a deep junction, for example, was found to produce stresses large enough to plastically deform silicon. A game of cat-and-mouse ensued; an unexpected effect, such as a rat bite, would cause catastrophic failure, and be traced to stress. A work-around would be developed to limit the stress to less than an appropriate threshold and the cycle would begin anew.

As the feature sizes in devices have become smaller and smaller, the problems caused by stress have multiplied and are now regarded as a routine part of doing business. Indeed, rather than trying to minimize stress, it is now being used to enhance specific attributes of devices. A prime example is the application of stress to the channel regions of metal-oxide–semiconductor field-effect transistors to enhance carrier mobility and hence device speed. This is the system that the CEMES–CNRS team uses to demonstrate the power of their approach for measuring strain.